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RADIO FREQUENCY MEMORIES

by

Zhou Goufu, Ji Guoliang

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DESIGN OF PHASE QUANTIZATION DIGITAL RADIO FREQUENCY MEMORIES

Zhou Goufu and Ji Guoliang
China Electronics System Engineering Company,
Beijing 100083

Abstract: This paper discusses the designs of the resistor-loop phaseshifter, input encoder, and output decoder used in a phase quantization digital radio frequency memories (DRFM), and analyzes the relationship between instantaneous bandwidth and sampling frequency of the phase quantization DRFM. The results show that the instantaneous bandwidth of the phase quantization DRFM is equal to, in numeral, the sampling frequency, which is the same as the I, Q double-channel amplitude quantization DRFM.

Keywords: Digital radio frequency memory, Phase quantization, Electronic warfare, Deception jammer, Computer simulation.

I. Introduction

As one of the key techniques of modern electronic warfare systems, the digital radio frequency memory (DRFM) technique began in the early seventies. After nearly two decades' efforts, the system has undergone great development with applications in many electronic warfare systems [1]. When designing DRFM systems, to overcome shortcomings of amplitude quantization DRFM (to eliminate the number of quantization digits, the properties of parasitic signals are sensitive to amplitude variation of

input signals), researchers proposed a phase quantization method. Based on the phase (not amplitude) of the input signal, quantization of the signal is carried out. The greatest advantage is that theoretically, the power level of the parasitic signals in the output signal is not affected by the input signal amplitude, therefore there is a great dynamic range of the signals.

As regards to the problem of executing the properties of phase quantization DRFM, and three-digit phase quantization DRFM, more detailed research was undertaken in the current literature [2, 3]. As a continuation of the above-cited work, this paper further penetratingly and systematically studies the problem of executing phase quantization DRFM.

II. Realization of 3-Digit Phase Quantization DRFM

From [3], we can obtain the block diagram as shown in Fig. 1 in executing the phase quantization DRFM. In the problem of executing comparators and adders, detailed presentations were given in [3]. So this paper does not repeat it. In the following, mainly the problems of executing compilers and decoders are presented.

In the 3-digit phase quantization DRFM, since the output from the comparator is 4-bit data flow (expressed, respectively, as $I_0 = \text{sgn}[\cos(\theta)]$, $I_1 = \text{sgn}[\cos(\theta - 45°)]$, $I_2 = \text{sgn}[\sin(\theta)]$, $I_3 = \text{sgn}[\cos(\theta + 45°)]$) . In the data flow, only eight states are affected, and there are another eight complement-states. To reduce the memory capacity requirement, compilation can be conducted on comparator output to 4-bit data flow converted to 3-bit data flow. Correspondingly,

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to obtain the required 4-bit data flow of the adder, after the data is removed from RAM, the data should be passed through a decoder to restore the 3-bit data flow into the original 4-bit data flow.

To carry out the functions of compiler and decoder, various multiple schemes can be applied, mainly determined by the extent of difficulties of circuit execution. Below is given a scheme for selection. The conversion relationship between the input
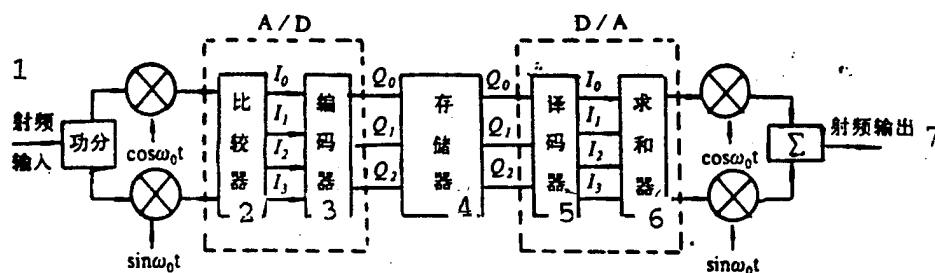
Fig. 1. Block diagram of 3-digit phase quantization DRFM
KEY: 1 – radio frequency input   2 – comparator
3 – compiler   4 – memory   5 – decoder   6 – adder
7 – radio frequency output   8 – division of functions

compiler and output decoder is (refer to Table 1):

$$Q_2 = I_0 \qquad\qquad I_0 = Q_2$$
$$Q_1 = I_2 \qquad\qquad I_2 = Q_1$$
$$Q_0 = I_1 + I_3 \qquad I_1 = Q_2 Q_1 Q_0 + Q_2 Q_1 Q_0 + Q_2 Q_1 Q_0 + Q_2 Q_1 Q_0$$
$$I_3 = Q_2 Q_1 Q_0 + Q_2 Q_1 Q_0 + Q_2 Q_1 Q_0 + Q_2 Q_1 Q_0$$

III. Execution of Multiple-digit Phase Quantization DRFM

Compared with 3-digit phase quantization, execution of multiple-digit phase quantization DRFM is much more complicated, mainly shown in the generation of comparator input signals, and the design of compiler/decoder.

1. Generation of comparator input signals

In the three-digit phase quantization system, the comparator input signal can be taken directly from I, Q as well as -I and -Q. However, when the number of quantization digits is greater than 3, the simple combinations of I, Q, as well as -I, -Q cannot be used to indicate the input signal of the comparator. Then the resistor-loop phase shifting method as presented below can be applied.

In this method, as shown in Fig. 2, the I, Q, -I and -Q signals are applied, respectively, at the four vertices of the resistor loop. However, the comparator input signals are taken

TABLE 1. Corresponding Relationship between I_0, I_1, I_2, I_3 as well as Q_0, Q_1, Q_3

Q_2	Q_1	Q_0	I_0	I_1	I_2	I_3
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	1	1	1
0	1	1	0	0	1	1
1	0	0	1	0	0	0
1	0	1	1	1	0	0
1	1	0	1	1	1	1
1	1	1	1	1	1	0

from the 2^{n-1} (here, n is the number of quantization digits) paired nodal points. Fig. 2 (a) and 2 (b) show, respectively, the structure of resistor-loop in the case of 3-digit quantization and 4-digit quantization.

As shown in Fig. 2, in the resistor-loop phase shifter, the number of resistors in each arm is 2^{n-2}. Because of symmetry, the number of resistors used for different resistance values is 2^{n-3}.

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Let $R = \sum R_i$, it is easy to derive the following working formula for various resistance values:

$$R_i = \frac{2R}{1 + \cot(i\theta)} - \sum_{j=1}^{i-1} R_j \qquad (i = 1,2,3,\cdots,N) \tag{1}$$

In the equation, $\theta = 45° / N$, $N = 2^{n-3}$. When the number of quantization digits is between 2 and 4, the calculation result of Eq. (1) is shown in Table 2.

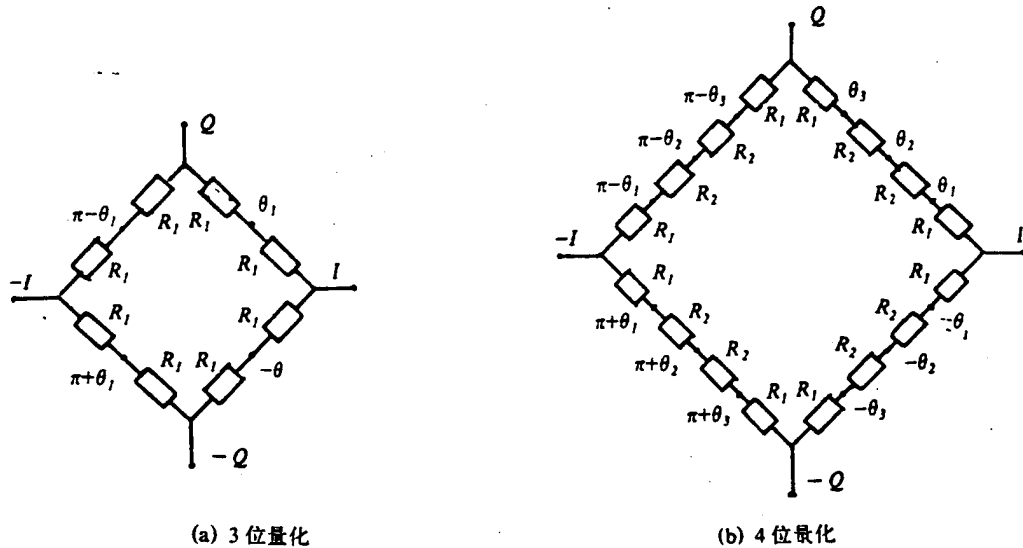(a) 3 位量化   (b) 4 位量化

Fig. 2. Resistor-loop phase shifter
KEY: (a) - 3-digit quantization
(b) - 4-digit quantization

2. Designs of compiler/decoder

Corresponding to n-digit phase quantization, there are 2^{n-1} comparators, corresponding to 2^n phases. Therefore, it is actually required to have the number of digits for storage to be n, not 2^{n-1}. Thus, at the comparator input and output terminals of memory, a compiler and decoder of 2^{n-1} to n digits, and n to 2^{n-1} are, respectively, required in order to have the n-digit memory and the 2^{n-1} comparator be matched with the adder. In the

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foregoing, there is the scheme for the execution of the compiler/decoder required in 3-digit phase quantization DRFM. By using a similar method, we can discover the scheme for executing the compiler/decoder required to execute multiple-digit quantization, but only more complicated. Therefore, no further description is made.

TABLE 2. Selection of Various Resistance Values in Resistor Loop

$$(\text{对} R = R_1 + R_2 + \cdots + R_2^{n-3} \text{归一化})$$

量化位数	电阻 阻 值			
n	R_1	R_2	R_3	R_4
3	1			
4	0.586	0.414		
5	0.332	0.254	0.215	0.199

KEY: 1 - (Normalization with respect to

2 - Number of quantization digits
3 - resistance values

IV. Relationship Between Instantaneous Bandwidth and Sampling Rate

As is well known, in the amplitude quantization DRFM system the sampling rate can be reduced by one-half compared with that of a single channel [4], to a certain instantaneous bandwidth, by processing the I and Q dual channel. Naturally, we would ask whether there is the same property as in amplitude quantization as dual channel processing is adopted in the phase quantization DRFM system. This is a problem of concern to all, and also a problem that should be solved before designing the phase

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quantization DRFM. Our answer is definite to this problem.
Based on reference [4], we can consider the signal previously
obtained as the I-channel signal (indicated by I_0, I_1, I_2, and I_3)
and its 90^0 phase-shifting signals can be indicated by I_2, $-I_3$,
$-I_0$, and I_1) as the Q-channel signals. Through orthogonal
modulation, we can obtain a similar relationship between the
instantaneous bandwidth and sampling rate in the dual-channel
amplitude quantization DRFM. As shown in Figs. 3 and 4, the
computer simulation results of the 3-digit quantization DRFM
system also verified this point.

The following parameters were selected in the computer
simulation process: pulse width $\tau=1\mu s$ and sampling frequency
$f_s=100MHz$. In Fig. 3, the input signal frequency f=77Mhz; three
sets of curves indicate signal waveforms in the range,
respectively, 0 to $0.1\mu s$, 0.45 to $0.55\mu S$, and 0.9 to $1.0\mu s$. In
these curves, the first in each curve set is the output
duplicating signals; and the second is the inputted original
signals. The simulation results are shown in Fig. 4 for the case
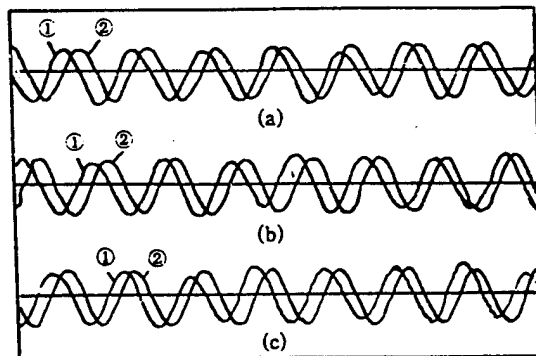when the input signal frequency is 92MHz.

Fig. 3. Simulation results of 3-digit phase
quantization DRFM
($\tau=1\mu s$, $f_s=100MHz$, f=77MHz)

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V. Conclusions

The paper discusses the problem of execution relating to phase quantization DRFM, and proposes a method of using resistor loop-phase shifters to generate the comparator input signals, and presents input compiler and output decoder of 3-digit phase quantization DRFM. The paper verified the relationship between the instantaneous bandwidth and sampling rate in phase quantization DRFM; verification was obtained by computer simulation. The following conclusions can be obtained from an analysis of the paper and by referring to other literature.
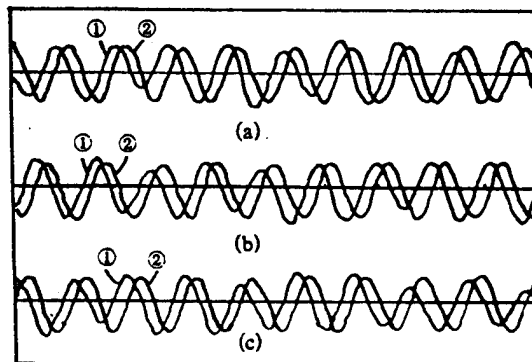
Fig. 4. Simulation of results of 3-digit phase quantization DRFM
($\tau=1\mu s$, $f_s=100MHz$, $f=92MHz$)

(1) By using the phase quantization method, the same instantaneous bandwidth of I and Q dual-channel amplitude quantization can also be obtained. In other words, this is numerically equal to the sampling frequency, but not one-half of the sampling frequency.

(2) Inherently, the power level of the parasitic signal of the output signal in phase quantization DRFM is not related to

the input signal amplitude. Therefore, the signal has great dynamic range.

(3) For 3-digit phase quantization DRFM, except for the two points mentioned above, since only four comparators are required, and since there is no requirement for resistor-loop phase shifter network, and the compilers/decoders are relatively simpler, therefore this is relatively easier to carry out. This is a scheme that can be selected at present to develop the DRFM products.

In addition, it is required to explain that for a 3-digit phase quantization system, when the requirements on memory capacity are not strict, it also can directly store the output 4-bit signal from the comparator, thus not requiring compiler/decoder, thereby simplifying the circuitry design.

The paper was received for publication on September 16, 1992.

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